WHAT IS CLAIMED IS:

1. A semiconductor apparatus having circuit components, comprising:

a first bus interconnecting the circuit components;

a second bus interconnecting the circuit components; and

a switching unit outputting a select signal that causes each circuit component to select one of the first bus and the second bus when transmitting a signal from one of the circuit components to another,

the second bus having a size larger than a size of the first bus.

2. A semiconductor apparatus having circuit components, comprising:

a first bus interconnecting the circuit components;

a second bus interconnecting the circuit components; and

a switching unit outputting a select signal that causes each circuit component to select one of the first bus and the second bus when transmitting a signal from one of the circuit components to another,

the second bus being provided in a second layer that is disposed above a first layer in which the first bus is provided.

3. A semiconductor apparatus having circuit components, comprising:

a first bus interconnecting the circuit components;

a second bus interconnecting the circuit components; and

a switching unit outputting a select signal that causes each circuit component to select one of the first bus and the second bus when transmitting a signal from one of the circuit components to another,

the switching unit being configured such that the first bus is selected only when a wafer test is conducted before formation of the second bus, and the second bus is selected at any time the semiconductor apparatus operates after the wafer test is conducted.

4. The semiconductor apparatus according to claim 1, wherein the first bus and the second bus are provided to transmit a same signal from one of the circuit components to another.

5. The semiconductor apparatus according to claim 1, wherein the first bus and the second bus are provided to transmit at least one of an address signal, a data signal, a control signal and a clock signal between the circuit components.

6. The semiconductor apparatus according to claim 1, wherein the first bus is provided for transmission of the signal between the circuit components before formation of the second bus, and, when the semiconductor apparatus operates before the formation of the second bus, the signal is transmitted on the first bus from one of the circuit components to another.

7. The semiconductor apparatus according to claim 1, wherein the switching unit is configured such that the second bus is always selected when the semiconductor apparatus operates after the formation of the second bus in the semiconductor apparatus.

8. The semiconductor apparatus according to claim 1, wherein the switching unit is provided to establish electrical connection between the circuit components by only the selected one of the first bus and the second bus.

9. The semiconductor apparatus according to claim 1, wherein the switching unit is provided with a programmable device.

10. The semiconductor apparatus according to claim 1, wherein the second bus includes signal line portions having a substantially equal length.

11. A semiconductor apparatus having circuit components, comprising:

a first wiring layer provided on a chip and including a number M of first electrodes, the M first electrodes being connected to the circuit components via a first bus; and

a second wiring layer provided above the first wiring layer

and including a number N of second electrodes, the N second electrodes being connected to the circuit components via a second bus, the second bus having a size larger than a size of the first bus,

wherein the semiconductor apparatus is configured such that a clock signal is received at each of the first electrodes and the second electrodes and the conditions $M > N \geqq 1$ are met.

12. The semiconductor apparatus according to claim 11, wherein the circuit components includes respective receiver units each of which is connected to one of the M first electrodes, and, when a select signal is set at a first level, the clock signal received at each first electrode is transmitted through the first wiring layer to corresponding one of the circuit components, and, when the select signal is set at a second level, the clock signal received at each second electrode is transmitted through the second wiring layer to corresponding one of the circuit components.

13. A multi-chip semiconductor apparatus in which a first chip and a second chip coexist and each of the first and second chips includes circuit components, one of the first and second chips comprising:

a first wiring layer provided on a semiconductor substrate;

a second wiring layer provided on an insulating layer covering the first wiring layer, the second wiring layer including conductive lines each interconnecting the circuit components of said one of the first and second chips;

a plurality of first electrodes provided in the first wiring layer; and

a second electrode provided on each of the conductive

lines, each conductive line being configured to interconnect the plurality of first electrodes and the second electrode.

14. A multi-chip semiconductor apparatus in which a first chip and a second chip coexist and each of the first and second chips includes circuit components, one of the first and second chips comprising:

a first wiring layer provided on a semiconductor substrate;

a second wiring layer provided on an insulating layer covering the first wiring layer, the second wiring layer including conductive lines each interconnecting the circuit components of said one of the first and second chips;

a first electrode provided in the first wiring layer; and

a plurality of second electrodes provided on each of the conductive lines, the conductive lines being configured to interconnect the first electrode and the plurality of second electrodes.

15. A multi-chip semiconductor apparatus in which a first chip and a second chip coexist and each of the first and second chips includes circuit components, one of the first and second chips comprising:

a first wiring layer provided on a semiconductor substrate;

a second wiring layer provided on an insulating layer covering the first wiring layer, the second wiring layer including conductive lines each interconnecting the circuit components of said one of the first and second chips;

a plurality of first electrodes provided in the first wiring layer; and

a plurality of second electrode provided on each of the conductive lines, the conductive lines being configured to

interconnect the plurality of first electrodes and the plurality of second electrodes.

16. The semiconductor apparatus according to claim 13, wherein the conductive lines include a loop-like conductive line connected to the circuit components of the first and second chips.

17. The semiconductor apparatus according to claim 15, wherein the plurality of second electrodes are provided such that, when the first and second chips are combined together, the plurality of second electrodes contact corresponding electrodes of the other of the first and second chips so that the conductive lines interconnect the first chip and the second chip via the plurality of second electrodes.

18. A multi-chip semiconductor apparatus in which a first chip and a second chip coexist and each of the first and second chips includes circuit components, one of the first and second chips comprising:

a first wiring layer provided on a semiconductor substrate;

a second wiring layer provided on an insulating layer covering the first wiring layer, the second wiring layer including conductive lines each interconnecting the circuit components of said one of the first and second chips;

a first electrode provided in the first wiring layer; and

a plurality of second electrodes provided on each of the conductive lines, the conductive lines being configured to

interconnect the first electrode and the plurality of second electrodes,

wherein the plurality of second electrodes are provided such that, when the first and second chips are combined together, the plurality of second electrodes contact corresponding electrodes of the other of the first and second chips so that the conductive lines interconnect the first chip and the second chip via the plurality of second electrodes.

19. A multi-chip semiconductor apparatus in which a plurality of chips coexist and each of the plurality of chips includes circuit components, comprising:

a first wiring layer provided on a semiconductor substrate;

a second wiring layer provided on an insulating layer covering the first wiring layer, the second wiring layer including conductive lines each interconnecting the circuit components of said one of the first and second chips;

a plurality of first electrodes provided in the first wiring layer; and

a plurality of second electrodes provided on each of the conductive lines, the conductive lines being configured to interconnect the plurality of first electrodes and the plurality of second electrodes.

20. A multi-chip semiconductor apparatus in which a first chip and a second chip coexist and each of the first and second chips includes circuit components, the first chip comprising:

a first wiring layer provided on a first semiconductor substrate;

a second wiring layer provided on a first insulating layer covering the first wiring layer, the second wiring layer

including first conductive lines each interconnecting the circuit components of the first chip;

a first electrode provided in the first wiring layer; and

a second electrode provided on each of the first conductive lines, each first conductive line being configured to interconnect the first electrode and the second electrode,

the second chip comprising:

a third wiring layer provided on a second semiconductor substrate;

a fourth wiring layer provided on a second insulating layer covering the third wiring layer, the fourth wiring layer including second conductive lines each interconnecting the circuit components of the second chip;

a third electrode provided in the third wiring layer; and

a fourth electrode provided on each of the second conductive lines, the fourth electrode being configured such that, when the first and second chips are combined together, the four electrode contacts the second electrode.

21. A multi-chip semiconductor apparatus in which a first chip and a second chip coexist and each of the first and second chips includes circuit components,

the first chip comprising:

a first wiring layer provided on a semiconductor substrate;

a second wiring layer provided on an insulating layer covering the first wiring layer, the second wiring layer including conductive lines each interconnecting the circuit components of the first chip;

a first electrode provided in the first wiring layer; and

a second electrode provided on each of the conductive lines, each conductive line being configured to interconnect the first electrode and the second electrode,

the second chip comprising:

a plurality of third electrodes which are configured such

when the first and second chips are combined together, the plurality of third electrodes contact the respective second electrodes of the first chip to interconnect the respective conductive lines of the first chip.

22. A multi-chip semiconductor apparatus in which a first chip and a second chip coexist and each of the first and second chips includes circuit components,

the first chip comprising:

a first wiring layer provided on a semiconductor substrate;

a second wiring layer provided on an insulating layer covering the first wiring layer, the second wiring layer including conductive lines each interconnecting the circuit components of the first chip;

a first electrode provided in the first wiring layer; and

a second electrode provided on each of the conductive lines, each conductive line interconnecting the first electrode and the second electrode,

the second chip comprising:

a plurality of third electrodes which are arranged such that, when the first and second chips are combined together, the plurality of third electrodes contact the respective second electrodes of the first chip so that the conductive lines form a loop-like large-size bus interconnecting the first chip and the second chip via the third electrodes.

23. A semiconductor apparatus comprising:

a first wiring layer provided on a semiconductor substrate;

a second wiring layer provided on a first insulating layer covering the first wiring layer, the second wiring layer including first conductive lines each interconnecting circuit

components of the semiconductor apparatus;

a first electrode provided in the first wiring layer; and

a second electrode provided within a contact hole of the first wiring layer, the first conductive lines interconnecting the first electrode and the second electrode, and

a second conductive line provided on a second insulating layer on the second wiring layer, the second conductive line interconnecting the second electrode and a third electrode provided within a contact hole of the first insulating layer.

24. A multi-chip semiconductor apparatus in which a plurality of chips are combined, each of the plurality of chips comprising:

a first wiring layer provided on a semiconductor substrate;

a second wiring layer provided on an insulating layer covering the first wiring layer, the second wiring layer including conductive lines interconnecting circuit components of the chip;

a first electrode provided in the first wiring layer; and

a plurality of second electrodes provided on the conductive lines for connection with an external device, each conductive line interconnecting the first electrode and the second electrodes, the second electrodes being arranged such that, when the plurality of chips are combined together, the second electrodes of the respective chips are connected to form a loop-like large-size bus interconnecting the plurality of chips via the second electrodes.

25. A multi-chip semiconductor apparatus in which a plurality of chips are combined, each of the plurality of chips comprising:

a first wiring layer provided on a semiconductor substrate;

a second wiring layer provided on an insulating layer covering the first wiring layer, the second wiring layer including conductive lines interconnecting circuit components of the chip;

a first electrode provided in the first wiring layer; and

a plurality of second electrodes provided on the conductive lines for connection with an external device, each conductive line interconnecting the first electrode and the second electrodes, the second electrodes being arranged such that, when the plurality of chips are combined together, the conductive lines of the respective chips are connected to form a plurality of large-size buses interconnecting the plurality of chips.

26. The semiconductor apparatus according to claim 13, wherein the conductive lines form a large-size bus.

27. The semiconductor apparatus according to claim 13, wherein the conductive lines form a bus that interconnects the circuit components of the semiconductor apparatus.

28. The semiconductor apparatus according to claim 13, wherein one of the first and second chips includes external connection electrodes, the external connection electrodes being disposed in peripheral portions of said one of the first and second chips which do not interfere with the other of the first and second chips.

29. A multi-chip semiconductor apparatus in which a first chip and a second chip are combined, comprising:

the first chip comprising an internal circuit and a plurality of electrodes connected to the internal circuit;

the second chip comprising:

a first wiring layer provided on a semiconductor substrate;

a second wiring layer provided on an insulating layer covering the first wiring layer, the second wiring layer including conductive lines each interconnecting circuit components of the second chip;

a plurality of first electrodes provided in the first wiring layer; and

a plurality of second electrodes provided on each of the conductive lines, the conductive lines being configured to interconnect the plurality of first electrodes and the plurality of second electrodes,

wherein the plurality of second electrodes are provided such that, when the first and second chips are combined together, the plurality of second electrodes contact the respective electrodes of the first chip so that the conductive lines interconnect the first chip and the second chip via the plurality of second electrodes.

30. The semiconductor apparatus according to claim 19, wherein the plurality of chips include a memory chip and a logic chip.

31. A semiconductor apparatus comprising:

an external terminal;

a first internal circuit connected to the external terminal via a first contact;

a second internal circuit connected to the external terminal via a second contact; and

a large-size bus connecting the external terminal to each of the first internal circuit and the second internal circuit,

wherein the large-size bus is provided in a second wiring layer on an insulating layer covering a first wiring layer provided on a semiconductor chip, the second wiring layer contacting both the first and second contacts, and the external terminal being brought into contact with the second wiring layer,

wherein the connection of the large-size bus enables the first internal circuit and the second internal circuit to be spaced apart each other.

32. A semiconductor apparatus comprising:

an external terminal;

a first internal circuit connected to the external terminal via a first contact;

a second internal circuit connected to the external terminal via a second contact; and

a large-size bus connecting the external terminal to each of the first internal circuit and the second internal circuit,

wherein the large-size bus is provided in a second wiring layer on an insulating layer covering a first wiring layer provided on a semiconductor chip, the second wiring layer contacting both the first and second contacts, and the external terminal being brought into contact with the second wiring layer,

wherein the large-size bus has a length larger than a permissible maximum length of a normal-size bus that is needed to attain protection of one of the first and second internal circuits, the normal-size bus being provided in the first wiring layer.

33. The semiconductor apparatus according to claim 31, further comprising a third internal circuit connected to the external terminal, the third internal circuit being disposed at an intermediate position between the first internal circuit and the second internal circuit.

34. The semiconductor apparatus according to claim 31, wherein the first internal circuit is a data input unit, and the second internal circuit is a data output unit.

35. A semiconductor apparatus comprising:

an external terminal;

an internal circuit connected to the external terminal via a first contact;

a circuit protecting device connected to the external terminal via a second contact;

a large-size bus connecting the external terminal to each of the internal circuit and the circuit protecting device, wherein the large-size bus is provided in a second wiring layer on an insulating layer covering a first wiring layer provided on a semiconductor chip, the second wiring layer contacting both the first and second contacts, and the external terminal being brought into contact with the second wiring layer.

36. The semiconductor apparatus according to claim 35, wherein the first wiring layer includes a first portion connecting the large-size bus and the internal circuit, and a second portion connecting the large-size bus and the circuit protecting device,

the first portion being larger than the second portion.

37. The semiconductor apparatus according to claim 35, wherein the semiconductor apparatus includes a resistor provided between the external terminal and the internal circuit.

38. The semiconductor apparatus according to claim 35, wherein the circuit protecting device is provided at a peripheral position of the semiconductor chip.

39. The semiconductor apparatus according to claim 31, wherein the large-size bus has a size larger than a size of a normal-size bus provided in the wiring layer.

40. The semiconductor apparatus according to claim 35, wherein the circuit protecting device is an electrostatic discharging device.

41. The semiconductor apparatus according to claim 31, wherein the external terminal is configured as the electrode directly contacting the second wiring layer.